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GAU 2181

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

(Case No. **RA001C11**)

In the Application of:

FARMWALD ET AL.

Serial No: 09/669,295

Filed: September 25, 2000

Title: METHOD OF OPERATION OF A MEMORY CONTROLLER

Group Art Unit: 2181

Before Examiner: G. Auve'

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231 on March 5, 2001

Michiko Sites
(Name of Person Mailing Correspondence)

Michiko Sites 3/5/01
Signature Date

Assistant Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

In compliance with the duty of disclosure set forth in 37 C.F.R. §1.56, submitted herewith is a modified Form PTO-1449, including a copy of all of the documents listed therein. An English translation has been obtained for one of the references and a copy of this translation is enclosed herewith.

Some of the references listed in the PTO-1449 have appeared in a communication from a foreign patent office in a related foreign application. A copy of that communication along with an English translation is also enclosed herewith.

It is respectfully requested that the Examiner make his consideration of the reference formally of record with the next Action. The Commissioner is hereby authorized to charge any fees which may be required in connection with this submission to Deposit Account No. 50-0998. A duplicate copy of this document is enclosed.

Respectfully submitted,

Date: March 2, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

CIPE SC169
MAR 13 2001
PATENT & TRADEMARK OFFICE

Ms. Michiko Sites
RAMBUS INC.
4440 El Camino Real
Los Altos, CA 94022

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Atty. Docket No. P001C11)

APPLICANT: **FARMWALD ET AL.** FILED: **SEPTEMBER 25, 2000**

SERIAL NO.: **09/669,295**

TITLE: **METHOD OF OPERATING A MEMORY CONTROLLER**

RECEIPT OF THE FOLLOWING PAPERS IS ACKNOWLEDGED

1. Information Disclosure Statement (1 page + 1 copy thereof + PTO-1449 (1 page)) + REFERENCES

DATE: **MARCH 5, 2001** ATTY: **NAS**

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UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

HYUNDAI ELECTRONICS INDUSTRIES CO., LTD., and HYUNDAI ELECTRONICS AMERICA Plaintiffs, v. RAMBUS, INC., Defendant.	Case No. C 00-20905 RMW **HYUNDAI'S INITIAL DISCLOSURE OF PRIOR ART UNDER LOCAL RULES 16-7 AND 16-8**

Pursuant to Rules 16-7 and 16-8 of the Local Rules of the U.S. District Court for the Northern District of California, Plaintiffs Hyundai Electronics Industries Co., Ltd. and Hyundai Electronics America (collectively "Hyundai") hereby make the present disclosure of prior art to Defendant Rambus, Inc. ("Rambus") of all claims believed to be asserted of U.S. Patent No. 5,915,105 ("the '105 patent"), U.S. Patent No. 6,101,152 ("the '152 patent"), U.S. Patent No. 6,038,195 ("the '195 patent"), U.S. Patent No. 6,032,214 ("the '214 patent"), U.S. Patent No. 6,032,215 ("the '215 patent"), U.S. Patent No. 5,953,263 ("the '263 patent"), U.S. Patent No. 6,035,365 ("the '365 patent"), U.S. Patent

No. 5,995,443 ("the '443 patent"), U.S. Patent No. 6,067,592 ("the '592 patent"), U.S. Patent No. 5,954,804 ("the '804 patent"), U.S. Patent No. 6,034,918 ("the '918 patent").

This disclosure is made without prejudice to Hyundai's right to obtain and present at trial or in pretrial proceedings such additional information as may be acquired through discovery or otherwise in this action. Specifically, Hyundai bases its present invalidity positions on Rambus' known allegations of infringement and related claims. Should Rambus assert additional claims, Hyundai reserves the right to supplement its invalidity contentions. Formal discovery is on-going and Hyundai's investigation is still underway. Moreover, the scope of prior art relevant in this case may be further altered or defined by the Court's ruling on claim construction. Hyundai therefore reserves the right to modify or add to this list at any time.

I. INITIAL DISCLOSURE OF PRIOR ART

A. LIST OF REFERENCES

	Patent #	Title	Inventor(s)/ Assignee(s)	Filing Date	Issue Date
1.	JP 61-72350	DATA TRANSFER CONTROL SYSTEM	Hashimoto, Shigeru; Nishimura, Naoyuki /Fujitsu, Ltd.	9/14/84	4/14/86
2.	JP 57-14922	MEMORY STORAGE DEVICE	Junichi Taguri /Hitachi, Ltd.	7/2/80	1/26/82
3.	JP 60-55459	BLOCK DATA TRANSFER AND STORAGE CONTROL METHOD	Yoshihiro Miyazaki /Hitachi, Ltd.	9/7/83	3/30/85
4.	JP 63-142445	MEMORY DEVICE	Yasushi Taguchi; Hiroshi Murata /Mitsubishi Electric Corporation	12/5/86	6/14/88
5.	JP 64-29951	STORAGE SYSTEM	Takashi Kumagai /Hitachi, Ltd.	7/24/87	1/31/89
6.	JP 56-82961	MEMORY CONTROL METHOD	Kunihiro Kawamasa /Fujitsu Ltd.	12/11/79	7/7/81
7.	JP 60-80193	MEMORY SYSTEM	Jun Hasegawa; Kazuhiko Honma /Hitachi Microcomputer Engineering Co., Ltd. /Hitachi, Ltd.	10/7/83	5/8/85
8.	EP 0218523	PROGRAMMABLE ACCESS MEMORY	Powell, Jon/ SGS Thomson Microelectronics	09/26/86	05/30/89
9.	EP 0282735	CLOCK SIGNAL SUPPLY SYSTEM	Masuda, Noboru; Kamikawal, Ryotaro; Yagyu, Masayoshi; Yamayoto, Masakazu; Itoh, Hiroyuki; Saito, Tatsuya/ Hitachi, Ltd.	02/11/88	09/21/88
10.	EP 0424774	CLOCK DISTRIBUTION SYSTEM AND TECHNIQUE	Ming-Yu Li, Gabriel/ National Semiconductor Corporation	10/15/90	05/02/91
11.	EP 0449052	PARITY TEST METHOD AND APPARATUS FOR A MEMORY CHIP	Hochstedler, Charles; Lyon, Terry; Proebsting, Robert; Wendell, Dennis L./ National Semicondcutor Corporation	03/15/91	03/29/90
12.	3,691,534	READ ONLY MEMORY SYSTEM HAVING INCREASED DATA RATE WITH ALTERNATE DATA READOUT	Andrew G. Veradi; Richard B. Rubenstein; Steven Radoff	11/4/70	9/12/72

	Patent #	Title	Inventor(s)/ Assignee(s)	Filing Date	Issue Date
13.	3,771,145	ADDRESSING AN INTEGRATED CIRCUIT READ-ONLY MEMORY	Patricia P. Wiener	2/1/71	11/6/73
14.	4,231,104	GENERATING TIME SIGNALS	St. Clair, Richard P./ Teradynce, Inc.	04/26/78	10/28/80
15.	4,317,623	MEMORY USED IN AUTOMATIC EXPOSURE CONTROL MECHANISM	Nobusawa, Tsukumo/ Asahi Kogaku Kohyo Company Limited	08/29/80	03/02/82
16.	4,330,852	SEMICONDUCTOR READ/WRITE MEMORY ARRAY HAVING SERIAL ACCESS	Donald J. Redwine; Lionel S. White, Jr.; G.R. Mohan Rao /Texas Instruments Incorporated	11/23/79	5/18/82
17.	4,445,204	MEMORY DEVICE	Yukihoro Nishiguchi	10/05/81	04/24/84
18.	4,466,127	ENTRY APPARATUS OF DIGITAL VALUE IN MEMORY	Tsutomu Ohgishi; Tadashi Sakurai /Sanyo Electric Co., Ltd.	5/16/79	8/14/84
19.	4,536,795	VIDEO MEMORY DEVICE	Hirota, Akira; Miyahara, Hiroyuki; Kosaka, Yohiteru/ Victor Company of Japan, Ltd.	02/04/83	08/20/85
20.	4,616,268	METHOD AND SYSTEM FOR INCREASING USE EFFICIENCY OF A MEMORY OF AN IMAGE REPRODUCING SYSTEM	Shida, Junji/ Dainippon Screen Mfg. Co., Ltd.	03/05/84	10/07/86
21.	4,629,909	FLIP-FLOP FOR STORING DATA ON BOTH LEADING AND TRAILING EDGES OF CLOCK SIGNAL	Cameron, Kelly B./ American Microsystem, Inc.	10/19/84	12/16/86
22.	4,631,659	MEMORY INTERFACE WITH AUTOMATIC DELAY STATE	John Hayne, II; John Schabowski /Texas Instruments Incorporated	4/1/85	12/23/86
23.	4,648,102	BUS INTERFACE DEVICE FOR A DATA PROCESSING SYSTEM	Riso, Vladimir; Kuhne, Roland/ International Business Machines Corp.	03/05/84	03/03/87
24.	4,663,735	RANDOM/SERIAL ACCESS MODE SELECTION CIRCUIT FOR A VIDEO MEMORY SYSTEM	Mark F. Novak; Karl M. Guttag /Texas Instruments Incorporated	12/30/83	5/5/87
25.	4,672,470	VIDEO SIGNAL RECORDING AND REPRODUCING APPARATUS	Takeshi Morimoto; Kunio Sekimoto; Seigo Asada /Matsushita Electric Industrial Co., Ltd.	12/20/84	6/9/87

	Patent #	Title	Inventor(s)/ Assignee(s)	Filing Date	Issue Date
26.	4,675,850	SEMICONDUCTOR MEMORY DEVICE	Masaki Kumanoya; Kazuyasu Fujishima; Hideshi Miyatake; Hideto Hidaka; Katsumi Dosaka; Tsutomu Yoshihara /Mitsubishi Denki Kabushiki Kaisha	6/25/85	6/23/87
27.	4,719,505	COLOR BURST REGENERATION	Ron D. Katznelson /M/A-COM Government Systems, Inc.; Cable/Home Communication Corp.	9/19/86	1/12/88
28.	4,754,433	DYNAMIC RAM HAVING MULTIPLEXED TWIN I/O LINE PAIRS	Daeje Chin; Wei Hwang; Nicky C. Lu /IBM Corporation	9/16/86	6/28/88
29.	4,825,287	DIGITAL VIDEO SIGNAL PROCESSOR	Baji, Toru; Matsuura, Tasuji; Tsukada, Toshiro; Ohba, Shinya/ Hitachi, Ltd.	06/18/87	04/25/89
30.	4,845,664	ON-CHIP BIT REORDERING STRUCTURE	Frederick J. Aichelmann, Jr.; Bruce E. Bachman /International Business Machines Corp.	9/15/86	6/4/89
31.	4,845,677	PIPELINED MEMORY CHIP STRUCTURE HAVING IMPROVED CYCLE TIME	Chappell, Barbara A.; Chappell, Terry I.; Schuster, Stanley E./ International Business Machines Corp.	08/17/87	07/04/89
32.	4,873,671	SEQUENTIAL READ ACCESS OF SERIAL MEMORIES WITH A USER DEFINED STARTING ADDRESS	Kowshik, Vikram; Boddu, Sudhakar; Lucero, Elroy M./ National Semiconductor Corporation	01/28/88	10/10/89
33.	4,876,670	VARIABLE DELAY CIRCUIT FOR DELAYING INPUT DATA	Takeo Nakabayashi; Masao Nakaya /Mitsubishi Denki Kabushiki Kaisha	12/9/87	10/24/89
34.	4,901,036	FREQUENCY SYNTHESIZER WITH AN INTERFACE CONTROLLER AND BUFFER MEMORY	Herold, Barry W.; Tahernia, Omid; Davis, Walter L.; Rivas, Mario A./ Motorola Inc.	06/29/89	02/13/90
35.	4,953,128	VARIABLE DELAY CIRCUIT FOR DELAYING INPUT DATA	Hiroyuki Kawai; Masahiko Yohsimoto/ Mitsubishi	12/16/87	08/28/90
36.	4,979,145	STRUCTURE AND METHOD FOR IMPROVING HIGH SPEED DATA RATE IN A DRAM	S. Remington; William Martino/ Motorola, Inc.	05/01/86	12/18/90
37.	5,009,481	OPTICAL MODULE AND METHOD OF MANUFACTORING SAME	Kinoshita, Kitoshi; Aoki, Hiroatsu/ Fujitsu Limited	08/23/89	04/23/91

	Patent #	Title	Inventor(s)/ Assignee(s)	Filing Date	Issue Date
38.	5,016,226	APPARATUS FOR GENERATING A DATA STREAM	Kiyokasu Hiwada; Nobuyuki Kasuga/ Hewlett Packard	11/09/88	05/14/91
39.	5,023,835	SEMICONDUCTOR MEMORY SYSTEM FOR USE IN LOGIC LSI'S	Akimoto, Kazuhiro; Oqiue, Katsumi; Uchiyama, Takeo/ Hitachi, Ltd.	05/10/89	06/11/91
40.	5,036,495	MULTIPLE MODE-SET FOR IC CHIP	Busch, Robert E.; Hovis, William P.; Redman, Theodore M.; Thoma, Endre P.; Yankosky, James A./ International Business Machines Corp.	12/28/89	07/30/91
41.	5,111,486	BIT SYNCHRONIZER	Oliboni, Mark L.; Woltz, Stephen H.; Drapac, George A.; Davis, Walter L./ Motorola Inc.	03/15/89	05/05/92
42.	5,123,100	TUNING CONTROL METHOD IN A COMMON BUS SYSTEM HAVING DELAY AND PHASE CORRECTING CIRCUITS FOR TRANFERRING DATA IN SYNCHRONIZATION AND TIME DIVISION SLOT AMONG A PLURALITY OF TRANSFERRING UNITS	I. Hisada; K. Takashi/ NEC	01/10/90	06/16/92
43.	5,142,376	IMAGE SIGNAL RECORDING AND REPRODUCING SYSTEM WITH PILOT SIGNAL PHASE-LOCKED WITH A SYNCHRONIZING SIGNAL	Tokihiko Ogura /Canon Kabushiki Kaisha	12/14/89	8/25/92
44.	5,206,833	PIPELINED DUAL PORT RAM	Shear-Jiung Lee/ Acer Inc.	03/13/91	04/27/93
45.	5,276,846	FAST ACCESS MEMORY STRUCTURE	Aichelmann Jr, Frederick J.; Bachmann, Bruce E.; Busch, Robert E.; Redman, Theodore M.; Thoma, Endre P./ International Business Machines Corp.	01/30/92	01/04/94
46.	reserved				
47.	5,301,155	MULTIBLOCK SEMICONDUCTION STORAGE DEVICE INCLUDING SIMULTANEOUS OPERATION OF A PLURALITY OF BLOCK DEFECT DETERMINATION CIRCUITS	Tomohisa Wada; Shuji Murakami /Mitsubishi Denki Kabushiki Kaisha	3/18/91	4/5/94
48.	5,301,278	FLEXIBLE DYNAMIC MEMORY CONTROLLER	R. Bowater; S. Larkey; J. St. Clair; P. Sidoli/ International Business Machines	04/23/92	04/05/95

	Patent #	Title	Inventor(s)/ Assignee(s)	Filing Date	Issue Date
49.	5,361,277	METHOD AND APPARATUS FOR CLOCK DISTRIBUTION AND FOR DISTRIBUTED CLOCK SYNCHRONIZATION	Wayne D. Grover /Alberta Telecommunications Research Centre	5/30/89	11/1/94
50.	5,684,753	SYNCHRONOUS DATA TRANSFER SYSTEM	Masahi Hashimoto; Gene A. Frantz; John Victor Moravec; Jean-Pierre Dolait /Texas Instruments Incorporated	6/7/95	11/4/97
51.	WO 89/12936	A METHOD OF ADJUSTING THE PHASE OF A CLOCK GENERATOR WITH RESPECT TO A DATA SIGNAL	Nordby, Rasmus/ NKT A/S	06/23/89	12/28/89
52.	4,998,262	GENERATION OF TOPOLOGY INDEPENDENT REFERENCE SIGNALS	Hans A.M. Wiggers /Hewlett-Packard Company	10/10/89	3/5/91
53.	5,361,277	METHOD AND APPARATUS FOR CLOCK DISTRIBUTION AND FOR DISTRUBUTED CLOCK SYNCHRNIZATION	Wayne Grover/ Alberta Telecommunications Research Centre	05/30/89	11/01/94
54.	JP 62-51509	METHOD FOR SETTLING MEMORY ACCESS TIMING	Tkahi Saito/		

55. K. Ohta, "**A 1-Mbit DRAM with 33-MHz Serial I/O Ports**", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986)
56. S. Watanabe et. al., "**An Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial Read/Write Mode**", IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 900-904 (Aug. 1989)
57. T. Yang, M. Horowitz, B. Wooley, "**A 4-ns 4Kx1-bit Two-Port BiCMOS SRAM**", IEEE Journal of Solid State Circuits, vol. 23, No. 5, pp. 1030-1040 (Oct. 1988)
58. Horowitz et al., "**MIPS-X: A 20-MIPS Peak 32-Bit Microprocessor with ON-Chip Cache**", IEEE J. Solid State Circuits, vol. SC-22, No. 5, pp. 790-798 (Oct. 1987)
59. T. Williams et. al., "**An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation**", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988)
60. K. Nogami et. al., "**A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC**", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990)
61. K. Numata et. al., "**New Nibbled -Page Architecture for High Density DRAM's**", IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 900-904 (Aug. 1989)
62. Robert J. Lodi et al., "**Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit,**" 1976 IEEE International Solid-State Circuits Conference (Feb. 18, 1976)
63. Robert J. Lodi et al., "**MNOS-BORAM Memory Characteristics,**" IEEE Journal of Solid-State Circuits, vol. SC-11, No. 5, pp. 622-631 (Oct. 1976)
64. Gregory Uvieghara et al., "**An On-Chip Smart Memory for a Data-Flow CPU,**" IEEE Journal of Solid-State Circuits, vol. 25, No. 1, pp. 84-89 (Feb. 1990)
65. Ray Pinkham et al., "**A 128Kx8 70-MHz Multiport Video RAM with Auto Register Reload and 8x4 WRITE Feature,**" IEEE Journal of Solid-State Circuits, vol. 23, no. 3, pp. 1133-1139 (Oct. 1988)
66. Hirotada Kuriyama et al., "**A 4-Mbit CMOS SRAM with 8-ns Serial-Access Time,**" 1990 Symposium on VLSI Circuits
67. David V. James, "**Scalable I/O Architecture for Buses,**" 1989 IEEE, pp. 539-544 (1989)
68. Takasugi, A. et al., "**A Data-Transfer Architecture for Fast Multi-Bit Serial Acess Mode DRAM,**" 11th European Solid State Circuits Conference, Tuolouse, France pp. 161-165 (Sep. 1985)

69. Amitai, Z., "**Burst Mode Memories Improve Cache Design,**" WESCON/90 Conference Record, pp. 29-32 (Nov. 1990)
70. Clement, Patrick, "**Process-Tolerant High Level Shifter,**" Motorola Technical Developments Publication, Vol. 7 (1987)
71. Fagan, J.L., "**A 16-kbit Nonvolatile Charge Addressed Memory,**" IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 5, pp. 631-636 (Oct. 1976)
72. Ikeda, Hiroaki et al., "**100 MHz Serial Acess Architecture for 4Md Field Memory,**" Symposium of VLSI Circuits, Digest of Technical Papers, pp. 11-12 (Jun. 1990)
73. Schmitt-Landsiedel, Doris, "**Pipeline Architecture for Fast CMOS Buffer RAMs,**" IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, pp. 741-747 (Jun. 1990)
74. Svensson, Christer, "**High Speed CMOS Chip to Chip Communication Circuit,**" IEEE International Symposium on Circuits and Systems, pp. 2228-2231 (Jun. 1991)
75. Wakayama, Myles, "**A 30-MHz Low-Jitter High-Linearity CMOS Voltage-Controlled Oscillator,**" IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 6, pp. 1074-1081 (Dec. 1987)
76. Whiteside, Frank, "**A Dual-Port 65ns 64Kx4 DRAM with a 50MHz Serial Output,**" IEEE International Solid-State Circuits Conference Digest (Feb. 1986)
77. Wu, Jich-Tsorng, "**A 100-MHz Pipelined CMOS Comparator,**" IEEE Journal of Solid-State Circuits, Vol. 23, No. 6, pp. 1379-1385 (Dec. 1988)
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81. Ishimoto, S. et al., "**A 256K Dual Port Memory**", ISSCC Digest of Technical Papers, p. 38-39 (Feb. 1985)
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83. Ohno, Chikai, "**Self-Timed: STRAM**", Fujitsu Sci. Tech. J., Vol. 24, No. 4, pp. 293-300 (Dec. 1988)
84. Schnaitter, William M. et al., "**A 0.5-GHz CMOS Digital RF Memory Chip**", IEEE Journal of Solid-State Circuits, vol. SC-21, no. 5, pp. 720-726 (Oct. 1986)
85. Bursky, Dave, "**Advanced Self-Timed SRAM Pares Access Time to 5 ns**", Electronic Design, pp. 145-147 (Feb. 22, 1990)
86. reserved
87. D. Wendell et al., "**A 3.5ns, 2Kx9 Self Timed SRAM**", 1990 IEEE Symposium on VLSI Circuits (Feb. 1990)
88. reserved
89. Tomoji Takada et al., "**A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Memories,**" IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989)
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91. Kanopoulos, Nick and Jill J. Hallenbeck, "**A First-In, First-Out Memory for Signal Processing Applications**", IEEE Transactions on Circuits and Systems, Vol. CAS-33, No. 5, pp. 556-558 (May 1986)
92. reserved
93. reserved

94.	4,788,667	SEMICONDUCTOR MEMORY DEVICE HAVING NIBBLE MODE FUNCTION	Masao, Nakano; Yohsihiro Takemae/ Fujitsu Limited	08/11/86	11/29/88

B. REFERENCE GROUPS

Group 1:

44, 45, 36, 40, 31, 37, 38, 22, 42, 23, 94, 32, 39, 41, 19, 49, 29, 15, 34, 11, 8, 10, 9, 51, 60, 58, 59, 66, 79, 80, 82, 68, 62, 63, 30, 24, 69, 72, 65, 73, 76, 35, 83, 55, 84, 61, 56, 33, 1, 50, 21, 12, 13, 17, 81, 5, 6, 7, 52, 53, 54, 16, 87, 89, 90, 91, 85

Group 2:

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Group 3:

36, 42, 23, 94, 39, 34, 11, 81, 82, 68, 62, 63, 30, 24, 65, 83, 33, 12, 13, 52, 53, 54, 16, 87, 85, 55, 56

Group 4:

44, 45, 36, 40, 31, 38, 17, 42, 23, 94, 19, 49, 29, 11, 8, 10, 82, 24, 72, 65, 73, 33, 5, 6, 7, 52, 53, 54, 16, 87, 89, 90, 91, 85, 55, 84, 56, 1, 50, 21, 12, 13

Group 5:

45, 36, 40, 17, 42, 23, 94, 29, 10, 60, 58, 72, 65, 73, 33, 5, 7, 16, 87, 90, 55, 84, 56

Group 6:

65, 5, 6, 7, 52, 16, 87, 89, 90, 91, 85, 83, 55, 84, 56

Group 7:

45, 23, 94, 39, 29, 11, 60, 58, 24, 72, 73, 74, 83, 33, 87, 90, 84, 56

Group 8:

44, 45, 36, 40, 31, 38, 17, 42, 23, 94, 11, 60, 58, 59, 66, 79, 62, 30, 24, 73, 74, 83, 55, 5, 6, 7, 52, 53, 54, 16, 87, 89, 90, 91, 85, 84, 64, 61, 56, 33, 1, 50, 21, 12, 13

Group 9:

44, 45, 36, 40, 31, 38, 17, 42, 23, 94, 11, 60, 58, 59, 66, 79, 62, 30, 24, 73, 74, 83, 55, 64, 5, 6, 7, 52, 53, 54, 16, 87, 89, 90, 91, 85, 84, 61, 56, 33, 1, 50, 21, 12, 13

Group 10:

23, 41, 19, 49, 29, 14, 20, 10, 9, 51, 18, 84, 64, 25, 27, 43, 52, 53, 89

Group 11:

37, 22, 17, 48, 8, 2, 5, 6, 7, 54, 90, 91

Group 12:

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Group 13:

37, 22, 17, 48, 8, 5, 6, 7, 54, 90, 91, 2

Group 14:

17, 48, 8, 5, 6, 7, 54, 90, 91, 2

Group 15:

12, 5

Group 16:

45, 40, 37, 94, 32, 8, 59, 66, 80, 62, 63, 30, 24, 70, 76, 67, 1, 3, 4, 13, 26

Group 17:

45, 36, 38, 94, 32, 47, 62, 30, 24, 65, 61, 56, 13, 55

Group 18:

45, 36, 37, 82, 62, 30, 24, 5, 6, 7, 16, 87, 90, 91, 85, 55, 84, 61, 56, 13

Group 19:

45, 36, 31, 38, 22, 17, 94, 32, 39, 19, 47, 11, 8, 60, 58, 59, 66, 79, 80, 81, 68, 62, 63, 30, 24, 69, 72, 65, 76, 83, 61, 56, 13, 5, 6, 7, 53, 54, 16, 87, 89, 90, 91, 85, 55, 50, 12

Group 20:

45, 36, 31, 38, 22, 17, 94, 32, 39, 19, 47, 11, 8, 60, 58, 59, 66, 79, 80, 81, 18, 68, 62, 63, 30, 24, 69, 72, 65, 76, 56, 50, 12, 13, 5, 6, 7, 53, 54, 87, 89, 90, 91, 85, 55

Group 21:

45, 36, 62, 30, 24, 28, 16, 84, 56

C. ANTICIPATION/OBVIOUSNESS

Where anticipation is indicated, reference is made to individual prior art references.

For obviousness, Hyundai has listed groups of references, set forth in Section B. This chart should be read as stating obviousness as any one of Group X in combination with any one of Group Y, etc....

1. The '105 Patent

Claims	Anticipated By Reference Nos.	Obvious In View Of A Combination Of The Following Groups
1	16, 55, 56	
2	16, 55, 56	
3	16, 55, 56	
4	16, 55, 56	
5	16, 55, 56	
6	16, 55, 56	References 16, 55 or 56 with Group 10
7	16, 55, 56	
8	16, 55, 56	
9		References 16, 55 or 56 with Group 7
10	90, 55, 45, 36, 5, 7, 16, 87, 56	2, 5, 18, 19
11	90, 55, 45, 36, 5, 7, 16, 87, 56	4, 18, 19
12	90, 55, 45, 36, 5, 7, 16, 87, 56	5, 18, 19
13		2, 5, 8, 10, 18, 19
14		3, 5, 8, 10, 18, 19
15	90, 55, 45, 36, 5, 7, 16, 87, 56	2, 5, 8, 18, 19
16	87	3, 5, 7, 8, 18, 19
17	16, 55, 56	
18	16, 55, 56	

19	16, 55, 56	
20	90, 55, 45, 36, 5, 7, 16, 87, 56	2, 5, 18, 19
21	87	3, 5, 7, 18, 19
22	87	3, 5, 7, 18, 19
23		3, 5, 8, 10, 18, 19
24	16, 55, 56	
25	16, 55, 56	
26	16, 55, 56	
27	16, 55, 56	
28	16, 55, 56	
29	16, 55, 56	
30	16, 55, 56	
31	5, 7, 55, 16, 87, 90, 45, 36, 94, 60, 58, 56	2, 5, 9, 19
32	90, 45, 36, 5, 7, 55, 16, 87, 56	2, 5, 9, 18, 19
33	45, 36, 16, 56	2, 5, 9, 19, 21
34		2, 5, 9, 10, 19
35		2, 5, 9, 10, 18, 19
36	53, 54, 87, 85, 55, 30, 24, 65, 12, 13, 63, 36, 94, 39, 11, 81, 68, 62, 56	3, 20
37	36, 94, 55, 56	3, 5, 9, 20
38	94, 55, 56	3, 5, 7, 9, 20
39	55, 56	3, 5, 7, 9, 20, 21
40		3, 5, 8, 10, 20
41		3, 5, 8, 10, 20
42		3, 5, 8, 10, 18, 20

43	36, 87, 55, 56	3, 5, 9, 18, 19
44		3, 5, 8, 9, 10, 18, 19
45		3, 5, 8, 9, 10, 18, 19

2. The '152 Patent

Claims	Anticipated By Reference Nos.	Obvious In View Of A Combination Of The Following Groups
1	5, 6, 7, 54, 90, 91, 37, 22, 17, 48, 8, 2, 12	11 - 15
2	5, 6, 7, 54, 90, 91, 37, 22, 8, 12	2, 11 - 15
3	5, 6, 7, 54, 90, 91, 37, 22, 8, 12	2, 11 – 15
4		2, 4, 10, 11 - 15
5	5, 6, 7, 54, 90, 91, 37, 22, 17, 48, 8, 2	11
6	12, 54	3, 11 - 15
7		3, 4, 10, 11 - 15
8		3, 5, 10, 11 - 15
9	37, 8	2, 11 – 15, 16
11	8, 5, 6, 7, 54, 90, 91	2, 8, 11 – 15, 19
12	8, 5, 6, 7, 54, 90, 91	2, 8, 11, 19
13	12, 54	3, 8, 11 – 15, 19
14	12, 54	3, 8, 11 – 15, 19
15	12, 54	3, 8, 11 – 15, 19
16		2, 4, 8, 10, 11 – 15, 18
17	5, 6, 7, 90, 91	2, 8, 11 – 15, 18
18	5, 6, 7, 54, 90, 91, 37, 22, 8, 12	2, 11 – 15

19	5, 6, 7, 54, 90, 91, 37, 22, 8, 12	2, 11
20	5, 6, 7, 54, 90, 91, 37, 22, 8, 12	2, 11, 13
21	22	2, 11, 12
22	12, 54	3, 11 – 15
23		3, 5, 11 – 15
24		2, 4, 10, 11 – 15
25		3, 5, 10, 11 – 15

3. The '195 Patent

Claims	Anticipated By Reference Nos.	Obvious In View Of A Combination Of The Following Groups
1	5, 6, 7, 54, 90, 91	2, 8, 9, 11, 20
2	5, 6, 7, 54, 90, 91	2, 4, 8, 11, 20
3	5, 6, 7, 54, 90, 91	2, 8, 11, 20
4		2, 4, 8, 10, 11, 20
5	5, 6, 7, 54, 90, 91	2, 8, 11, 13, 20
6	5, 6, 7, 54, 90, 91	2, 8, 11, 20
7	5, 6, 7, 54, 90, 91	2, 8, 11, 20
8	5, 6, 7, 54, 90, 91	2, 8, 11, 13, 20
9		2, 4, 8, 10, 11, 13, 20
10	5, 6, 7, 54, 90, 91	2, 8, 11, 13, 20
11	91, 5, 6, 7, 54, 90	2, 8, 11
12	5, 6, 7, 54, 90, 91	2, 4, 8, 9, 11, 19
13	5, 6, 7, 54 90, 91	2, 4, 8, 9, 11, 19
14		2, 4, 8, 10, 11
15	5, 6, 7, 54, 90, 91	2, 8, 11, 14
16	5, 6, 7, 54, 90, 91	2, 8, 11

17	5, 6, 7, 54, 90, 91	2, 8, 11
18	5, 6, 7, 54, 90, 91	2, 8,11, 13
19		2, 4, 8, 10, 11
20	5, 6, 7, 54, 90, 91	2, 8, 11, 13
21	5, 6, 7, 54, 90, 91	2, 4, 8, 9, 11, 19
22	5, 6, 7, 54, 90, 91	2, 4, 8, 9, 11, 19
23	5, 6, 7, 54, 90, 91, 37, 22, 8	2, 11
24	5, 6, 7, 54 90, 91, 8	2, 11, 14
27	22	2, 11, 12
32	5, 6, 7, 54, 90, 91, 37, 22, 8	2, 11
33	5, 6, 7, 90, 91	2, 6, 11
34	5, 6, 7, 54, 90, 91	2, 8, 11, 20
35	5, 6, 7, 54, 90, 91, 22, 8	2, 11, 20
36	5, 6, 7, 54, 90, 91, 22, 8	2, 11, 20
37	5, 6, 7, 54 90, 91, 22, 8	2, 11, 20
38	5, 6, 7, 54, 90, 91, 22, 8	2, 11, 20
39	5, 6, 7, 54, 90, 91, 22, 8	2, 11, 20

4. The '214 Patent

Claims	Anticipated By Reference Nos.	Obvious In View Of A Combination Of The Following Groups
1	94, 62, 63, 30, 24, 13	3, 16
2	94, 62, 63, 30, 24,	3, 16

	13	
3	94, 62, 63, 30, 24, 13	3, 16
4		3, 11,16
5		3, 11, 14, 16
6	94, 62, 63, 30, 24, 13	3, 16
9	94, 62, 63, 30, 24, 13	3, 16
10	94, 24, 62, 63, 30, 13	3, 4, 16
11		3, 4, 10, 16
12		3, 5, 10, 16
13		3, 5, 10, 16, 18
15	94, 62, 63, 30, 24, 13	3, 16
16	94, 62, 63, 30, 24, 13	3, 16
17	94, 62, 63, 30, 24, 13	3, 16
18		3, 11, 16
19		3, 11, 12, 16
20		3, 11, 14, 16
21	94, 62, 63, 30, 24, 13	3, 16
24		3, 6, 16
25	94, 24	3, 4, 16
26		3, 4, 10, 16
27		3, 5, 10, 16
28		3, 5, 10, 16
30		3, 11, 16
31		3, 11, 16
36		3, 11, 12, 16

37		3, 11, 14, 16

5. The '215 Patent

Claims	Anticipated By Reference Nos.	Obvious In View Of A Combination Of The Following Groups
1	36, 55	3, 5, 8, 9, 17, 18, 20
2		3, 5, 8, 9, 11, 17, 18, 20
3		3, 5, 8, 9, 10, 17, 18, 20
4		3, 5, 8, 9, 10, 17, 18, 20
5		3, 5, 8, 9, 10, 17, 18, 20
6		3, 5, 8, 9, 11, 17, 18, 20
7	36, 55	3, 5, 8, 9, 17, 18, 20
8	36, 55	3, 5, 8, 9, 17, 18, 20
9	36, 55	3, 5, 8, 9, 17, 18, 20
10	36, 55	3, 5, 8, 9, 17, 18, 20
11	36, 55	3, 5, 8, 9, 17, 18, 20
12	36, 55	3, 5, 8, 9, 17, 18, 20
13	36, 55	3, 5, 8, 9, 17, 18, 20
14		3, 5, 8, 9, 16, 17, 18, 20
17	36, 55	3, 5, 8, 9, 17, 18, 20
18		3, 5, 8, 9, 11, 17, 18, 20
19		3, 5, 8, 9, 10, 17, 18, 20
20		3, 5, 8, 9, 10, 17, 18, 20
21		3, 5, 8, 9, 11, 14, 17, 18, 20
22	36, 55	3, 5, 8, 9, 17, 18, 20
23	36, 55	3, 5, 8, 9, 17, 18, 20
24	36, 55	3, 5, 8, 9, 17, 18, 20

25	36, 55	3, 5, 8, 9, 17, 18, 20
26	36, 55	3, 5, 8, 9, 17, 18, 20
27	36, 55	3, 5, 8, 9, 17, 18, 20
28	36, 55	3, 5, 8, 9, 17, 18, 20
29		3, 5, 8, 9, 10, 17, 18, 20
30		3, 5, 8, 9, 10, 17, 18, 20
31		3, 5, 8, 9, 11, 14, 17, 18, 20
32	36, 55	3, 5, 8, 9, 17, 18, 20
35	36, 55	3, 5, 8, 9, 17, 18, 20
36	36, 55	3, 5, 8, 9, 17, 18, 20

6. The '263 Patent

Claims	Anticipated By Reference Nos.	Obvious In View Of A Combination Of The Following Groups
1	5, 6, 7, 54, 90, 91, 37, 22, 17, 48, 8, 2	11
2	5, 6, 7, 54, 90, 91, 22, 8	11, 2, 20
3	5, 6, 7, 54, 90, 91, 22, 8	11, 2, 20
4	22	11, 12
5	5, 6, 7, 54, 90, 91, 17, 48, 8	11, 14
6	5, 6, 7, 54, 90, 91, 37, 22, 17, 48, 8, 2	11
7	5, 6, 7, 54, 90, 91, 37, 22, 17, 48, 8, 2	11
8	5, 6, 7, 54, 90, 91, 37, 22, 17, 48, 8, 2	11

9	5, 6, 7, 54, 90, 91, 37, 22, 17, 48, 8, 2	11, 13
10	5, 6, 7, 54, 90, 91, 37, 22, 17, 48, 8, 2	11
11	22	11,12
12	5, 6, 7, 54, 90, 91, 17, 48, 8	11, 14
14	5, 6, 7, 54, 90, 91, 22, 8	2, 11, 20
15	5	2, 11, 15, 20
16	22	2, 11, 12, 20
17	5, 6, 7, 54, 90, 91, 8	2, 11, 14, 20
18	5, 6, 7, 54, 90, 91, 37, 22, 17, 48, 8, 2	11
19	5, 6, 7, 54 90, 91, 17, 48, 8	11, 14
21	22	11, 12, 14
23	22	11, 12, 13
24	5, 6, 7, 54, 90, 91, 37, 22, 17, 88, 8, 2	11
25	5, 6, 7, 54, 90, 91, 37, 22, 17, 88, 8, 2	11
26	5, 6, 7, 54, 90, 91, 37, 22, 17, 88, 8, 2	11
27	5, 6, 7, 54, 90, 91, 37, 22, 8	2, 11
28	11, 8, 5, 6, 7, 54, 90	2, 11, 14
30	5, 6, 7, 54, 90, 91, 22, 27, 8	1, 11, 20
31	5	1, 11, 15, 20

32	22	1, 11, 12, 19
33	5, 6, 54, 90, 91,	1, 11, 14, 19

7. **The '365 Patent**

Claims	Anticipated By Reference Nos.	Obvious In View Of A Combination Of The Following Groups
1	54	3, 8, 11, 19
2	54	3, 4, 8, 9, 11, 19
3	54	3, 4, 8, 9, 10, 11, 19
4	54	3, 4, 8, 10, 11, 19
5		3, 4, 7, 8, 10, 11, 19
6		3, 5, 8, 10, 11, 19
7		3, 5, 7, 8, 10, 11, 19
8		3, 5, 8, 10, 11, 19
9		3, 5, 8, 10, 11, 18, 19
11		3, 5, 8, 10, 11, 17, 19
12		3, 8, 11, 15, 19
13	54	3, 8, 11, 19
14	54	3, 8, 11, 19
15	54	3, 8, 11, 19
16	54	3, 8, 11, 19
17	54	3, 8, 11, 19
18	54	3, 8, 11, 19
20		3, 6, 8, 11, 19
21	54	3, 8, 11, 13, 19
22	54	3, 11, 20
23		3, 4, 10, 11, 20

24		3, 4, 10, 11, 20
25		3, 4, 10, 11, 20
26		3, 5, 9, 11, 20
27		3, 5, 9, 10, 11, 20
28		3, 5, 9, 10, 11, 20
29		3, 5, 10, 11, 20
30		3, 5, 10, 11, 20
31		3, 5, 11, 20, 21
32		3, 5, 11, 18, 20
33		3, 11, 15, 20
34		3, 11, 20, 21
35	54	3, 11, 20
36	54	3, 11, 20
37	54	3, 11, 20
38	54	3, 11, 20
39	54	3, 11, 20
40	54	3, 11, 20
42		3, 6, 11, 20
43	54	3, 11, 20
44	54	3, 11
46		3, 11, 12
47		3, 11, 15
48	54	3, 11, 14

8. **The '443 Patent**

Claims	Anticipated By Reference Nos.	Obvious In View Of A Combination Of The Following Groups
1	45, 36, 55	2, 5, 8, 9, 17, 18, 20
2	45, 36, 55	2, 5, 8, 9, 17, 18, 20
3		2, 5, 8, 9, 10, 17, 18, 20
4	45	2, 5, 7, 8, 9, 17, 18, 20
5	45, 36, 55	2, 5, 8, 9, 17, 18, 20
6		2, 5, 8, 9, 11, 17, 18, 20
7		2, 5, 8, 9, 11, 15, 17, 18, 20
8	45, 36, 55	2, 5, 8, 9, 17, 18, 20
9	45, 36, 55	2, 5, 8, 9, 17, 18, 20
10	45, 36, 55	2, 5, 8, 9, 17, 18, 20
12	45, 36, 55	2, 5, 8, 9, 17, 18, 20
13	45, 36, 55	2, 5, 8, 9, 17, 18, 20
14	45, 36, 55	2, 5, 8, 9, 17, 18, 20
15	45, 36, 55	2, 5, 8, 9, 17, 18, 20
16	55	2, 5, 6, 8, 9, 17, 18, 20
17	45, 36, 55	2, 5, 8, 9, 17, 18, 20
18	45	2, 5, 8, 9, 16, 17, 18, 20
21	45, 36, 55	2, 5, 8, 9, 17, 18, 20
22		2, 5, 8, 9, 10, 17, 18, 20
23		2, 5, 8, 9, 10, 17, 18, 20
24	45, 36, 55	2, 5, 8, 9, 17, 18, 20
25	45, 36, 55	2, 5, 8, 9, 17, 18, 20
26	45, 36, 55	2, 5, 8, 9, 17, 18, 20
27	45, 36, 55	2, 5, 8, 9, 17, 18, 20

28	45, 36, 55	2, 5, 8, 9, 17, 18, 20
29	45, 36, 55	2, 5, 8, 9, 17, 18, 20
30		2, 5, 8, 9, 10, 17, 18, 20
31		2, 5, 8, 9, 11, 15, 17, 18, 20
32	45, 36, 55	2, 5, 8, 9, 17, 18, 20
36	45, 36, 55	2, 5, 8, 9, 17, 18, 20
37	45, 36, 55	2, 5, 8, 9, 17, 18, 20

9. **The '592 Patent**

Claims	Anticipated By Reference Nos.	Obvious In View Of A Combination Of The Following Groups
1		2, 8, 11
2		2, 8, 11. 15
3		2, 8, 11
4		2, 8, 11, 20
11		2, 5, 8, 11, 20
13		2, 5, 8, 11, 20
15		3, 5, 8, 10, 11, 20
17		3, 5, 8, 9, 10, 11, 20
18		3, 5, 8, 9, 10, 11, 18, 20
19		3, 5, 8, 9, 10, 11, 18, 20
21	91, 90, 5, 6, 7, 54	2, 8, 11
22	91, 90, 5, 6, 7, 54	2, 8, 11
23		2, 8, 11, 16
24	5, 6, 7, 53, 90, 91	2, 8, 11, 20
29	5, 7, 90	2, 5, 8, 9, 11, 20

30	5, 7, 90	2, 5, 8, 9, 11, 18, 20
32	5, 6, 7, 54, 90, 91	2, 4, 8, 9, 11, 20
34		2, 4, 8, 9, 10, 11, 20
35	5, 6, 7, 54, 90, 91, 37, 22, 8, 12	2, 11
36	5, 6, 7, 54, 90, 91 22, 8	2, 11, 20
38		2, 4, 10, 11, 20
39		3, 5, 10, 11, 20

10. The '804 Patent

Claims	Anticipated By Reference Nos.	Obvious In View Of A Combination Of The Following Groups
26		3, 10, 11, 20

11. The '918 Patent

Claims	Anticipated By Reference Nos.	Obvious In View Of A Combination Of The Following Groups
1	45, 40, 37, 94, 32, 8, 59, 66, 80, 62, 63, 30, 24, 76, 1, 13	2, 16
2	45, 40, 37, 94, 32, 8, 59, 66, 80, 62, 63, 30, 24, 76, 1, 13	2, 16
3	45, 40, 37, 94, 32, 8, 59, 66, 80, 62, 63, 30, 24, 76, 1, 13	2, 16
6	45, 40, 37, 94, 32, 8, 59, 66, 80, 62, 63, 30, 24, 76, 1, 13	2, 16

7	45, 40, 37, 94, 32, 8, 59, 66, 80, 62, 63, 30, 24, 76, 1, 13	2, 16
8	37, 8	2, 11, 16
9	37, 8	2, 11, 16
10		2, 11, 15, 16
18	45, 40, 37, 94, 32, 8, 59, 66, 80, 62, 63, 30, 24, 76, 1, 13	2, 16
19	45, 40, 37, 94, 32, 8, 59, 66, 80, 62, 63, 30, 24, 76, 1, 13	2, 16
20	45, 40, 37, 94, 32, 8, 59, 66, 80, 62, 63, 30, 24, 76, 1, 13	2, 16
21	45, 40, 37, 94, 32, 8, 59, 66, 80, 62, 63, 30, 24, 76, 1, 13	2, 16
24	37, 8	2, 11, 16
25	37, 8	2, 11, 13, 16
26		2, 11, 13, 15, 16
29	45, 40, 37, 94, 32, 8, 59, 66, 80, 62, 63, 30, 24, 76, 1, 13	2, 16
31		2, 6, 16
33		2, 4, 10, 16
34		2, 6, 11, 16
35		2, 6, 11, 16
38		2, 6, 11, 15, 16

D. ADDITIONAL REFERENCES PRESENTLY UNDER INVESTIGATION

The following references are currently being reviewed by Hyundai. Hyundai will promptly supplement its prior art disclosure upon completion of its review.

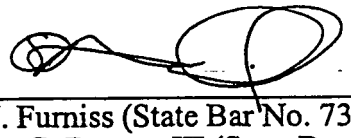
	Patent	Title	Inventor(s)/ Assignee(s)	Filing Date	Issue Date
95.	JP 63-217452	Setting System for Memory Access Timing	Saito Takashi/ Mitsubishi Electric Corp.	03/06/87	09/09/88
96.	4,691,302	Circuit Arrangement Comprising a Matrix-Shaped Memory Arrangement for Variably Adjustable Delay of Digital Signals	Hans J. Mattausch/ Siemens Aktiengesellschaft	07/28/86	09/01/87
97.	4,769,778	Circuit Arrangement Comprising a Matrix-Shaped Memory Arrangement for Digital Filtration of Image Signals in Row and Column Directions	Reinhard Tielert; Bernd Zehner/ Siemens Aktiengesellschaft	02/21/86	09/06/88
98.	4,740,924	Circuit Arrangement Comprising a Matrix-Shaped Memory Arrangement for Variably Adjustable Time Delay of Digital Signals	Rienhard Tielert/ Siemens Aktiengesellschaft	02/12/86	08/26/88
99.	4,785,428	Programmable Memory Array Control Signals	Atiq Bajwa; Robert Duzett; M. Vittal Kini; Kent Mason; Mark S. Myers; Sunil Shenoy/ Intel Corp.	06/18/87	11/15/88
100.	4,785,415	Digital Data Buffer and Variable Shift Register	Richard K. Karlquist/ Hewlett-Packard Company	08/29/86	11/15/88
101.	5,006,982	Method of Increasing the Bandwidth of a Packet Bus by Reordering Reply Packets	Ronald J. Ebersole; David Johnson; David Budde; Mark S. Myers; Gerhard Bier/ Siemens Aktiengesellschaft	10/21/88	04/09/91

	Patent	Title	Inventor(s)/ Assignee(s)	Filing Date	Issue Date
102.	4,858,113	Reconfigurable Pipelined Processor	Raymond J. Saccardi/ The United States of America as Represented by the Director of the National Security Agency	04/10/87	08/15/89
103.	4,637,018	Automatic Signal Delay Adjustment Method	Laurence P. Flora; Michael A. McCullough/ Burroughs Corp.	08/29/84	01/13/87
104.	5,021,985	Variable Latency Method and Apparatus for Floating - Point Coprocessor	Larry Hu; Ting Chuk; John McLeod; Mark Birman; Allen Samuels; George K. Chu/ Weitek Corp.	01/19/90	06/04/91
105.	4,322,635	High Speed Serial Shift Register for MOS Integrated Circuit	Donald J. Redwine/ Texas Instruments Incorporated	11/23/79	03/30/82
106.	4,636,986	Separately Addressable Memory Arrays in a Multiple Array Semiconductor Chip	Raymond Pinkham/ Texas Instruments Incorporated	01/22/85	01/13/87
107.	4,928,265	Semiconductor Integrated Circuit	Hisayuki Higuchi; Noriyuki Homma; Makoto Suzuki; Sugura Tachibana/ Hitachi Ltd.	11/02/88	05/22/90
108.	4,866,675	Semiconductor Memory Circuit Having a Delay Circuit	Shoichiro Kawashima/ Fujitsu Limited, Japan	08/05/88	09/12/89
109.	4,628,489	Dual Address RAM	Richard H. Ong; Peter C. Enconomopoulos; Russel W. Guenthner/ Honeywell Information Systems Inc.	10/03/83	12/09/86
110.	4,849,937	Digital Delay Unit with Interleaved Memory	Masahiko Yoshimoto/ Mitsubishi Deaki Kabushiki Kaisha	03/17/88	07/18/89

	Patent	Title	Inventor(s)/ Assignee(s)	Filing Date	Issue Date
111.	5,001,672	Video RAM with External Select of Active Serial Access Register	Timothy J. Ebbers; Satish Gupta; Randall L. Henderson; Nathan R. Hiltebeitel; Robert Tamlya; Steven W. Tomashot; Todd Williams/ International Business Machines Corp.	05/16/89	03/19/91
112.	5,261,064	Burst Access Memory	David C. Wyland/ Advanced Micro Devices Inc.	09/08/92	11/09/93
113.	4,315,308	Interface Between a Microprocessor Chip and Peripheral Subsystems	Daniel K. Jackson/ Intel Corp.	12/21/78	02/09/82
114.	4,849,937	Digital Delay Unit With Interleaved Memory	Masahiko Yoshimoto/ Mitsubishi Deaki Kabushki Kaisha	03/17/88	07/18/89
115.	EP 0334552	Semiconductor File Memory and Storage System Using the Same	Mikio Matoba; Ken Sugawara; Shigeru Sakairi/ Hitachi Maxell Ltd.	03/16/89	09/27/89
116.	4,712,190	Self-Timed Random Access Memory Chip	Paul M. Guglielmi; Ronald J. Melanson; Alan Kotok/ Digital Equipment Corp.	01/25/85	12/08/87
117.	4,876,670	Variable Delay Circuit For Delaying Input Data	Takeo Nakabayashi; Masao Nakaya/ Mitsubishi Denki Kabushiki Kaisha	12/09/87	10/24/89
118.	4,882,712	Synchronous Semiconductor Memory Device	Chikai Ohno; Michiyuki Hirata/ Fujitsu Limited, Kawasaki; Fujitsu VLSI Limited	09/26/88	11/21/89
119.	5,111,386	Cache Contained Type Semiconductor Memory Device And Operating Method Therefor	Kazuyasu Fujishima; Charles A. Hart/ Mitsubishi Denki Kabushiki Kaisha	06/14/90	05/05/92

DATED: October 13, 2000

Respectfully submitted,



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and HYUNDAI ELECTRONICS AMERICA

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PROOF OF SERVICE

I hereby certify and declare under penalty of perjury that the following statements are true and correct:

1. I am over the age of 18 years and am not a party to the within cause. My business address is 379 Lytton Avenue, Palo Alto, California 94301.

2. I am familiar with my company's mail collection and processing practices, know that said mail is collected and deposited with the United States Postal Service on the same day it is deposited in interoffice mail, and know that postage thereon is fully prepaid.

3. Following said practice, on October 13, 2000, I served by United States mail, a true copy of the attached document titled exactly **HYUNDAI'S INITIAL DISCLOSURE OF PRIOR ART UNDER LOCAL RULES 16-7 AND 16-8** by placing it in an addressed, sealed envelope and depositing it in regularly maintained interoffice mail to the following:

Cecilia H. Gonzalez
Joseph P. Lavelle
Basil C. Culyba
HOWREY SIMON ARNOLD & WHITE, LLP
1299 Pennsylvania Avenue, N.W.
Washington, D.C. 20004

Evangelina M. Almirantearena
HOWREY SIMON ARNOLD & WHITE, LLP
301 Ravenswood Avenue
Menlo Park, CA 94025

EXECUTED this13th day of October, 2000, at Palo Alto, California.

Sanya Edward

Sanya Edwards